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BY: Carrie Parker

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SPECIFICATION

To all whom it may concern:

Be It Known, That We, Sean Christopher Erickson, a citizen of the United States of America, residing at 2918 Sagebrush Drive, Fort Collins, Colorado 80525, Kevin Roy Nunn, a citizen of the United States of America, residing at 729 Parkview Drive, Fort Collins, Colorado 80525, and Jonathan Alan Shaw, a citizen of the United States of America, residing at 5025 Sawhill Drive, Fort Collins, Colorado 80528, have invented certain new and useful improvements in "High Performance Diode Implanted Voltage Controlled P-Type Diffusion Resistor", of which We declare the following to be a full, clear and exact description:

BACKGROUND OF THE INVENTION

1. Technical Field:

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The present invention relates generally to an improved circuit system and in particular to a resistor. Still more particularly, the present invention relates to a precision voltage controlled diffusion resistor.

2. Description of the Related Art:

A resistor is an electrical device that may convert energy into heat. The letter R is used to denote the resistance value of a resistor. With this device, two possible reference choices are present for the current and voltage at the terminals of the resistor. One is current in the direction of the voltage drop across the resistor and another is the current in the direction of voltage rise across the resistor.

Some existing problems with respect to resistors include transmission line impedance mismatching (caused by line width variations through etching), the physical size required for diffusion resistors, and process variation in diffusion resistors. Currently, existing solutions for these problems include special Microwave Integrated Circuit (MIC) processes to make trimmed resistors. This type of process involves using a laser to trim the resistors. The resistance is measured and a laser is used to reduce the size of the resistor. This type of process requires much time and is expensive to perform on a per circuit basis. Alternatively, high-precision discrete components are soldered or bonded to an integrated circuit (IC) or package. These currently used solutions are expensive with respect to the manufacturing of semiconductors. Further, these existing solutions are difficult to integrate into a silicon IC process because of the size of components and/or specialized manufacturing requirements needed to trim the devices. Further, discrete or trimmed components are not adjustable after the manufacture of a product.

Therefore, it would be advantageous to have an improved diffusion resistor that overcomes the problems of the existing solutions.

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SUMMARY OF THE INVENTION

The present invention provides a p-type diffusion resistor that is formed in the substrate. A p-type diffusion region is formed within the substrate that contains first and second p+ contact regions at either end of the diffusion region to form the two ends of the diffusion resistor. Third and fourth contact regions, both n+ regions, are located within the diffusion region between the first and second contacts and on either side of the conduction channel between the two end points. The third and fourth contacts form diodes such that the application of a voltage to these contacts causes respective depletion regions surrounding the contacts. All of the contacts are connected to metal layers overlying the resistor. The depletion regions surrounding the third and fourth contacts change in size depending on the voltage applied to their respective contacts. Increasing the size of the depletion regions increases the resistance of the depletion resistor by narrowing the conduction channel between the two contacts.

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BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself however, as well as a preferred mode of use, further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figure 1A is a view looking down on the surface of a voltage-controlled diffusion resistor after the regions have been implanted but before contacts are added, in accordance with a preferred embodiment of the present invention;

Figures 1B-1D are cross-sections of the voltage controlled diffusion resistor of Figure 1A, shown after contacts have been formed. These figures demonstrate contacts with a salicide on the substrate under the contact for both diodes and endpoints of the resistor;

Figures 2A-2G are diagrams illustrating the cross-section of the resistor shown in Figure 1C at various processing steps for creating the resistor in accordance with a preferred embodiment of the present invention; and

Figure 3 is a schematic diagram of a radio frequency (RF) driver or receiver circuit with RF feedback in accordance with a preferred embodiment of the present invention.

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DETAILED DESCRIPTION

The present invention provides for an improved diffusion resistor that is voltage controlled. The illustrative embodiment of the present invention takes advantage of the fact that there exists a depletion region, a volume of the semiconductor devoid of charge carriers, whenever two oppositely doped concentrations come together. The depletion layer that results in the semiconductor may be used in conjunction with a voltage bias on the diode to reduce or increase the effective resistance of a diffusion resistor.

The structure of a high-precision voltage controlled diffusion resistor in the illustrative embodiments of the present invention includes a low mobility diffusion region with a positive contact at one end and a negative contact at the opposite end. The low mobility diffusion region defines a conduction channel. Near the center of the resistor, the sides of the conduction channel are defined by the two diodes, formed by a metal-to-silicon contact and an N-type doped implant. The negative and positive contact regions are typical ohmic contacts.

The resistance is made variable in these depicted examples through providing an ability to tune the resistor through voltage-controlled contacts (VCC) to each of the diodes. When the VCC contact is biased, the thickness of the depletion region is changed, which in turn changes the width of the conduction channel. As a result, an increase or decrease in effective resistance in the structure is created depending on the particular voltage applied to the VCC contact. In this manner, an ability to vary the resistance of the diffusion resistor through a voltage bias is accomplished.

The reduction in the conduction width allows the creation of a resistor of a higher value in the same space as a diffusion resistor that does not use a diode contact. This in turn provides for a reduction in physical resistor size. This advantage is accomplished in the depicted examples as explained here: A basic diffusion resistor has a conduction width "t", which is directly related to the amount of current it will conduct. In the innovative resistor, this width "t" is reduced by "2·d", where d is the width of each depletion region. Thus, the diffusion resistor of the present invention has a conduction thickness of "t - (2·d)". In these examples, the VCC may be tied to ground and an increase in the effective resistance still exists.

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Advantages of the disclosed resistor include the ability to make a smaller resistor, to modulate the value of the resistor after manufacturing, to simplify the manufacturing of resistors of a given resistance. The resistance value can be elevated to an extreme value and can be used as a fail safe circuit.

The processes, steps, and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as necessary for an understanding of the present invention. The figures below represent cross sections of a portion of an integrated circuit during fabrication and are not drawn to scale, but are drawn so as to illustrate the important features of the invention.

With reference now to the figures and in particular with reference to Figure 1A, a top view of voltage-controlled diffusion resistor 100 is depicted in accordance with a preferred embodiment of the present invention. The resistor is formed in elongated region 102 of silicon substrate that has been lightly doped with a p-type dopant. The p-type dopant can be, for example, boron. Regions of heavier doping 104 and 106 at each end of resistor 100 provide positive and negative terminals of the resistor. Two n+ regions 108 and 110 are formed near the center of the resistor and define between them channel 112 through which a current can flow from one terminal to the other. The n+ contact regions form diodes and cause depletion regions 138 and 140 to form around them. The size of depletion regions 138 and 140 can be increased or decreased by the application of appropriate voltages.

Figure 1B-1D show cross-sections of voltage-controlled diffusion resistor 100 of
Figure 1A, after contacts have been formed. Because n+ regions 108 and 110 do not extend
across the entire width of resistor 100, Figure 1B, which looks at a section extending down the
midline of the resistor, shows only p+ contact regions 104 and 106, while Figure 1C, which
looks at a section offset from the midline, shows both p+ regions 104 and 106 and n+ regions
108 and 110. Figure 1D, which looks at a section through the midpoint of resistor 100 taken
perpendicular to the section of Figure 1B, shows only n+ regions 108, 110. Contact 124 and
contact 126 for the terminals are formed on salicided regions 114 and 116. Salicided region 108

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(not shown) is formed on n+ contact region 118 (also not shown), and salicided region 110 is formed on n+ contact region 120. These contacts are standard ohmic contacts formed by metal layers. Contact 104 in this example is a positive terminal for diffusion resistor 100, while contact 106 forms a minus terminal for diffusion resistor 100. Contacts 108 and 110 are voltage control contacts (VCC) for a diode. In this example, contact 130 is formed over salicided region 120 and contact area 110. Depending on the voltage bias applied to contact 110, depletion region 140 is formed and may grow or shrink.

Figure 1E is an enlargement of the central region of Figure 1D, showing the distances that are important in terms of the depletion regions. As voltage is applied to contacts 128 and 130, depletion regions 138 and 140 grow in size. In particular, "d" represents the width of each of depletion regions 138 and 140. This value increases as voltage is applied to contacts 128 and 130. In this example, "t" represents the width of channel 112 and also represents the conductivity. The overall conductivity is "t - 2d" in which the conductivity decreases as d increases with the size of depletion regions 138 and 148.

Turning now to **Figures 2A-2G**, these diagrams illustrate cross-sections taken along the same line as for **Figure 1C** during processing steps for creating the voltage controlled diffusion resistor in accordance with the preferred embodiments of the present invention. In **Figure 2A**, the resistor **100** is formed in a p-well that has been previously formed. In a less preferred embodiment, the well can also be an n-well. To begin formation of the resistor, a layer of resist **RST** is deposited over the substrate, which includes the n-well or p-well. The resist is patterned and developed to expose the region where the resistor will be formed, but remains intact over adjacent regions. A p-type dopant is implanted into the device. In this example, the dopant may be, for example, boron. The implant is performed to result in a low concentration of p-type dopants. These dopants in these examples have a concentration of about 1×10^{13} per cm³ or greater. The doping profile of p-diffusion region **102** may be tuned in these examples to reduce parasitic capacitance.

In Figure 2B, the previous photo resist layer has been removed and a new layer of resist RST has been deposited. This layer of resist has been developed to make a pattern that exposes those areas where the end terminals of the resistor will be. The device is then implanted with

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additional p-type dopant to create a high concentration of n-type dopants in contact regions 204 and 206. Typically, the concentration may range from 1×10^{18} per cm³ to 1×10^{20} per cm³.

In Figure 2C, the existing resist layer has again been removed and a new resist RST deposited and patterned to expose diode contact regions 208 and 210. An n-type dopant, such as arsenic or phosphorus, is implanted. Typically, the concentration can range from $1x10^{18}$ per cm³ to $1x10^{20}$ per cm³.

In Figure 2D, a new layer of resist RST is developed to expose contact regions 204, 206, 208, and 210 in the resistor. A refractory metal, such as titanium or cobalt, is deposited to form a thin layer over the exposed silicon regions, seen here as 214', 216', and 220'. The chip is then heated in a rapid thermal anneal process, which causes the refractory metal to react with the silicon substrate to form metal salicide regions 214, 216, 218, and 220, as seen in Figure 2E.

After the salicide contacts are formed, a layer of an insulator, known as an interlevel dielectric ILD, is deposited. This layer can be composed of, for example, silicon dioxide, SiO₂. Preferably, the dielectric layer ILD is planarized using chemical mechanical processing (CMP), forming the structure of Figure 2E. A resist (not shown) will be formed over the interlevel dielectric layer. The resist will be patterned using the same pattern previously used to determine where the refractory metal for the salicide would be deposited. The dielectric layer is then etched to remove the dielectric over the contact areas, forming the structures seen in Figure 2F. Finally, a refractory metal such as tungsten is deposited into the contact regions thus exposed to form contacts 124, 126, 128, and 130, seen in Figure 2G.

Notably, in these examples, lengths "L1" and "L2" of Figure 1C and the width "t" of Figure 1E are typically minimized in order to maximize the effect of the depletion regions on the total resistance. Preferably, the dimensions of the resistor are designed so that the depletions would not touch. However, even if the two depletion regions did touch, the substrate would provide enough carriers for some current flow, so that the device is always in the linear region.

Turning now to **Figure 3**, a schematic diagram of a Rf driver or receiver circuit with RF feedback is depicted in accordance with a preferred embodiment of the present invention. In these examples, the RF feedback employs a variable resistor, such as the variable resistor in the illustrated examples. In this example, circuit **300** includes current source **302**, transistor **304**,

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resistor 306, and resistor 308. In these examples, resistor 306 is an Rd resistor connecting transistor 304 to ground. Current source 302 has one end connected to transistor 304 and another end connected to voltage source VDD. Further, transistor 304 and current source 302 are connected to Vout. Vin is connected to the gate of transistor 304 and resistor 308. In these examples, resistor 308 is a variable diffusion resistor as illustrated in the depicted examples.

Thus, the present invention in the illustrated examples provides for an adjustable or tunable resistance value in a diffusion resistor. The absolute value of the resistor in these examples may be modified with a voltage bias on the metal contact of the diode. By changing the voltage bias, the thickness of the depletion region may be increased or decreased. With this feature, impedance matching adjustment for radio frequency (Rf) driver/receiver circuits may be made. The voltage controlled diffusion resistor in the illustrated examples allows for adjustment of the resistor value Rin for a receiver application or Rout for a driver application to match the transmission line impedance. In this manner, unwanted voltage reflections and signal loss are reduced or eliminated.

Further, adjustments to resistance allow for a bias current adjustment for mixed signal circuits. Also, the reduction in the size of the resistor is accomplished by reducing the resistor thickness. Additionally, resistance values may be self-adjusting through various circuit design techniques, such as implementing a feedback circuit with the resistor of the present invention. Further, the variable resistance value may be adjusted to compensate for process variations to provide for uniform resistance. Also, the variable resistance may be adjusted to a very high resistance to put an analog circuit in a low current or low power sleep mode.

The description of the preferred embodiment of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art. The embodiment was chosen and described in order to best explain the principles of the invention the practical application to enable others of ordinary skill in the art to understand the invention for various embodiments with various modifications as are suited to the particular use contemplated.